Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-15. (Cancelled)

16. (New) A method for synchronizing a regularly occurring pulse train in frequency to the average of a bunched pulse train, the method comprising:

generating from an oscillator a plurality of differently phase shifted regularly occurring pulse trains at a given frequency;

selecting one of the regularly occurring pulse trains;

filling a FIFO with the bunched pulse train;

emptying the FIFO at the frequency of the selected regularly occurring pulse train;

generating an error signal that represents the state of the FIFO;

filtering the error signal;

accumulating the filtered error signal to produce a phase selection signal; and

changing the selected regularly occurring pulse train responsive to the phase selection signal so the selected regularly occurring pulse train is at the average frequency of the bunched pulse train.

17. (New) The method of claim 16, in which generating a plurality of differently phase shifted pulse trains comprises connecting a plurality of differential amplifier stages in tandem and coupling the differential amplifier stages together to form a ring oscillator, the regularly occurring phase shifted pulse trains being generated by the respective stages such that each stage produces two pulse trains shifted in phase 180□ from each other.

18. (New) The method of claim 17, in which the coupling couples together differential amplifier stages that have equal controllable delays.

19. (New) The method of claim 18, in which the coupling couples eight differential amplifier stages together such that sixteen differently phase shifted pulse trains are generated.

20. (New) The method of claim 19, in which the accumulating accumulates the filtered error signal at the frequency of the regularly occurring pulse train..

21. (New) The method of claim 16, in which the regularly occurring pulse trains have two binary values and the changing changes from one regularly occurring pulse train to another regularly occurring pulse train when both regularly occurring pulse trains have the same binary value.

22. (New) The method of claim 16, in which the generating a plurality of differently phase shifted pulse trains comprises synchronizing the oscillator to a stable frequency reference.

23. (New) The method of claim 22, in which the synchronizing comprises incorporating in a phase locked loop a number of counters with programmable dividing factors that determine the frequency of the phase shifted pulse trains and programming the counters to establish the desired frequency.

24. (New) The method of claim 23, in which the phase locked loop has a broad bandwidth.

25. (New) The method of claim 24, in which the filtering comprises providing a control loop that has a narrow bandwidth.

26. (New) The method of claim 16, additionally comprising adding a frequency offset to the filtered error signal prior to accumulating the filtered error signal.

27. (New) The method of claim 26, in which the frequency offset is selected to minimize the correction made by selecting one of the regularly occurring pulse trains.

28. (New) A method for synchronizing a regularly occurring clock pulse train in frequency to the average of a bunched clock pulse train corresponding to data, by use of a FIFO having a given number of storage locations, an empty flag storage cell

for each location, and a full flag storage cell for each location, the method comprising:

generating as an output signal the regularly occurring clock pulse train;

filling the FIFO with the data responsive to the bunched clock pulse train and emptying the FIFO responsive to the output signal;

setting an empty flag in an empty flag storage cell of a storage location and resetting a full flag in the full flag storage cell of the storage location when data is read out of the corresponding storage location;

setting a full flag in the full flag storage cell of a storage location and resetting an empty flag in the empty flag storage cell of the storage location when data is written into the corresponding storage location;

summing either the empty flags or the full flags to produce an error signal that represents the state of the FIFO; and

changing the frequency of the output signal responsive to the error signal so the state of the FIFO remains approximately constant.

29. (New) The method of claim 28, additionally comprising adding a frequency offset to the error signal before the error signal changes the frequency of the output signal.

30. (New) The method of claim 29, in which the frequency offset is selected to minimize the correction made to the output signal.